01/11/99

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Check Box, if applicable [ ] Duplicate

Attorney Docket No.	970150A	Total Pages	

First Named Inventor or Application Identifier

Yasunori INOUE

Express Mail Label No.

PAGE 1 OF 3

APPLICATION ELEMENTS FOR:

SEMICONDUCTOR DEVICE INCLUDING AN INSULATION FILM ON A CONDUCTIVE LAYER AND MANUFACTURING METHOD THEREOF

ADDRESS TO: Assistant Commissioner for Patents
BOX PATENT APPLICATIONS
Washington, D.C. 20231

1. [X] Fee Transmittal Form (Incorporated within this form)
(Submit an original and a duplicate for fee processing)

2. [X] Specification Total Pages [35]

3. [X] Drawing(s) (35 USC 113) Total Sheets [9]

4. [X] Oath or Declaration Total Pages [2]

a. [ ] Newly executed (original or copy)

b. [X] Copy from prior application (37 CFR 1.63(d) (for continuation/divisional with Box 17 completed).

i. [ ] Deletion of Inventor(s)
Signed statement attached deleting inventor(s) named in prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. [ ] Incorporation by reference (usable if box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. [ ] Microfiche Computer Program (Appendix)

7. [ ] Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

a. [ ] Computer Readable Copy
b. [ ] Paper Copy (identical to computer copy)
c. [ ] Statement Verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [ ] Assignment Papers (cover sheet and document(s))

9. [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [X] Power of Attorney

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	970150A
First Named Inventor or Application Identifier	Yasunori INOUE
	PAGE 2 OF 3

10. [ ] English translation Document (if applicable)
11. [X] Information Disclosure Statement [ ] Copies of IDS Citations
12. [X] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503)
14. [ ] Small Entity Statement(s) [ ] Statement filed in prior application Status still proper and desired.
15. [X] Claim for Convention Priority [ ] Certified copy of Priority Document(s)
    a. Priority of Japanese application no. 8-043679 filed on February 29, 1996 and Japanese application no. 9-012788 filed on January 27, 1997 are claimed under 35 USC 119. The certified copies have been filed in prior application Serial No. 08/806,425.
16. [ ] Other _____
17. [X] If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

    [ ] Continuation [X] Division [ ] Continuation-in-part (CIP) of prior application no. 08/806,425

    a. [X] Please amend the specification by inserting after the title: --This application is a division of prior application Serial No. 08/806,425 filed February 26, 1997.--

    b. [X] Cancel in this application original claims 1-8 of the prior application before calculating the filing fee.

FEE TRANSMITTAL The filing fee is calculated below	Number Filed	Number Extra	Rate	Basic Fee $760.00
Total Claims	10 - 20		x $18.00	
Independent Claims	2 - 3		x $78.00	
Multiple Dependent Claims			$260.00	
			Basic Filing Fee	$760.00
Reduction by 1/2 for small entity				
Fee for recording enclosed Assignment			$40.00	
TOTAL				$760.00

UTILITY PATENT APPLICATION TRANSMITTAL (Only for new nonprovisional applications under 37 CFR 1.53(b))	Attorney Docket No.	970150A
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	Yasunori INOUE	
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[X] A check in the amount of $760.00 is enclosed to cover the filing fee.

[ ] Please charge our Deposit Account No. **01-2340** in the total amount of $___ to cover the filing fee and the $__ assignment recordation fee. A duplicate of this sheet is attached.

[X] The Commissioner is hereby authorized to charge payment for any additional filing fees required under 37 CFR 1.16 or credit any overpayment to Deposit Account No. **01-2340**. A duplicate of this sheet is attached.

18. CORRESPONDENCE ADDRESS

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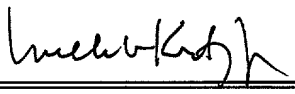
Signature		Date: January 11, 1999

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Yasunori INOUE

Serial Number: [Division of 08/806,425]

Filed: January 11, 1999

For: SEMICONDUCTOR DEVICE INCLUDING AN INSULATION FILM ON A CONDUCTIVE LAYER AND MANUFACTURING METHOD THEREOF

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

January 11, 1999

Dear Sir:

Prior to action on the above-identified application, please amend the same as follows:

IN THE SPECIFICATION:

Change the title to read --METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE--.

Page 2, line 9: after "which" insert --a--;

line 12: after "having" insert --a--.

Page 9, delete lines 23-25 and substitute therefor:

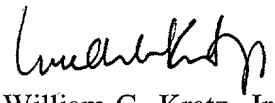
--Fig. 16 is a sectional view of the structure of a semiconductor device where a spacer is omitted from the structure shown in Fig. 1 in order to describe effects of the spacer.--

REMARKS

The present amendment corrects language which was corrected and entered in parent application Serial No. 08/806,425 to provide conformity between the present divisional application and the parent application.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI,
McLELAND & NAUGHTON



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TITLE OF THE INVENTION

Semiconductor Device Including an Insulation Film on a Conductive Layer and Manufacturing Method Thereof

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to semiconductor devices and a manufacturing method thereof, and more particularly, to a semiconductor device having an insulation film on a conductive layer, and a manufacturing method thereof.

Description of the Background Art

Reducing the size of interconnections and providing multilayers thereof are now required to further increase the integration density of semiconductor integrated circuit devices. It is necessary to insert an interlayer insulation layer between each interconnection to provide a multilayer structure of the interconnections. If the surface of this interlayer insulation layer is not planar, a stepped portion will be generated at the interconnection formed above the interlayer insulation film. This causes defects such as disconnection.

Therefore, the surface of the interlayer insulation film (the surface of the device) must be made as flat as possible. The technique to planarize the surface of the device is called planarization. This planarization

technique has become important in reducing the size and providing multilayers of the interconnection.

An SOG (Spin On Glass) film is known as an interlayer insulation film commonly used in planarization. Research of this SOG film is particularly in progress in the planarization technology taking advantage of fluidity of the material of the interlayer insulation film.

An "SOG film" is a generic term of a film mainly composed of a solution in which silicon compound is dissolved in an organic solvent, and silicon dioxide (SiO_2) formed from that solution.

In forming an SOG film, first a solution having silicon compound dissolved in an organic solvent is applied on a substrate in droplets. The substrate is rotated. By this rotation, the solution coating is provided on the substrate formed of interconnections so as to alleviate the stepped portion thereon. More specifically, the coating is formed thick at the concave portion and thin at the convex portion on the substrate. Thus, the solution coating is planarized at the surface.

Heat treatment is then applied to vaporize the organic solvent. Also, polymerization proceeds to result in a planarized SOG film at the surface.

An SOG film is typically classified into an inorganic SOG film that does not include any organic component of a

silicon compound, as represented by the following general formula (1), and an organic SOG film including an organic component in a silicon compound, as represented by the following general formula (2).

$[SiO_2]n$ ...(1)

$[R_xSiO_Y]n$ ...(2)

(n, X, Y : integer; R: alkyl group or aryl group)

Inorganic SOG contains a great amount of moisture and a hydroxyl group. The inorganic SOG has a disadvantage that it is more brittle than a silicon oxide film formed by CVD (Chemical Vapor Deposition). For example, a crack is easily generated during heat treatment in an inorganic SOG film when thicker than 0.5μm.

In contrast, an organic SOG film has the generation of a crack during heat treatment suppressed. The organic SOG film can be formed having a thickness of approximately 0.5-1.0μm. The usage of an organic SOG film allows the formation of an interlayer insulation film that is greater in film thickness. Therefore, sufficient planarization can be achieved for even a great stepped portion on a substrate.

Although superior in planarization, an inorganic SOG film may adversely affect the metal interconnection and the like since it contains a great amount of moisture and a hydroxyl group. There is a possibility of degradation in

the electric characteristics, corrosion, and the like. This problem may similarly be encountered in an organic SOG film including, though smaller in amount than the inorganic SOG film, moisture and a hydroxyl group.

Therefore, when an SOG film is employed as an interlayer insulation film, an insulation film such as a silicon oxide film formed by plasma CVD, for example, having the property of blocking moisture and hydroxyl groups as well as having high insulation and mechanical strength is generally provided above or below the SOG film.

A silicon oxide film formed by plasma CVD is superior in water resistance than an SOG film. However, it was conventionally difficult to obtain satisfactory water resistance effect even when a silicon oxide film formed by plasma CVD is applied. It was therefore difficult to improve reliability of a semiconductor device such as insulation characteristics while also improving planarization in conventional art.

SUMMARY OF THE INVENTION

An object of the present invention is to improve planarization as well as reliability of a semiconductor device.

Another object of the present invention is to achieve superior planarization and insulation characteristics in a semiconductor device.

A further object of the present invention is to easily manufacture a semiconductor device superior in planarization and insulation characteristics in a manufacturing method of a semiconductor device.

According to an aspect of the present invention, a semiconductor device includes a first insulation film, and a film for substantially preventing intrusion of impurities into a conductive layer. The first insulation film is formed on the conductive layer, and includes impurities. The film preventing intrusion is formed between the first insulation film and the conductive layer. By forming the first insulation film including impurities on the conductive layer, the first insulation film is modified to have the moisture and the hydroxyl group reduced. The first insulation film becomes less hygroscopic. Therefore, the water resistant ability of the first insulation film is improved. By using an SOG film, for example, as the first insulation film, both planarization and water resistance can be improved. Furthermore, the provision of a film between the first insulation film and the conductive layer effectively prevents the impurities of the first insulation film from entering the conductive layer. The disadvantage of a shorter electromigration lifetime of the conductive layer before disconnection due to intrusion of the impurities of

the first insulation layer into the conductive layer can be prevented. The film for preventing intrusion can include at least one material selected from the group consisting of silicon oxide, silicon nitride, Ti, TiN, W, WN_X and TiW. A second insulation film may be included between the first insulation film and the conductive layer. The second insulation film can be formed to include a film that is less hygroscopic than the first insulation film. Also, the first insulation film may include silicon oxide containing at least 1% of C (carbon). The first insulation film may further include an inorganic SOG film. The impurities may include at least one element selected from the group consisting of argon, boron, nitrogen, and phosphorus. The upper surface of the first insulation film may be planarized.

According to a method of manufacturing a semiconductor device of another aspect of the present invention, a first insulation film is formed on a conductive layer on a substrate. Impurities are introduced into the first insulation film. Prior to formation of the first insulation film, a film for preventing intrusion of impurities of the first insulation film into the conductive layer is formed on the conductive layer. According to the manufacturing method of a semiconductor device of the present aspect, first insulation film is

modified by introducing impurities into the first insulation film. As a result, the moisture and the hydroxyl group included in the first insulation film are reduced. The first insulation film is now less hygroscopic. Thus, a first insulation film superior in water resistance can be obtained. By using an SOG film as the first insulation film, planarization is also improved. Thus, a semiconductor device that can be improved both in planarization and water resistance can be manufactured. By providing a film between the conductive layer and the first insulation film, intrusion of impurities from the first insulation film into the conductive layer can be prevented effectively. Therefore, the disadvantage of the impurities entering the conductive layer to adversely affect the lifetime thereof can be prevented. The film for preventing intrusion can be formed including at least one material selected from the group consisting of silicon oxide, silicon nitride, Ti, TiN, W, WN_X and TiW. In the above-described structure, a step can be included of forming a second insulation film on the conductive layer and the film preventing intrusion prior to the step of forming the first insulation film. In this case, the second insulation film can include a film less hygroscopic than the first insulation film. Also, a step can be included of forming a third insulation film on the first

insulation film after the step of implanting impurities into the first insulation film. The first insulation film can include silicon oxide consisting at least 1% of C, or an inorganic SOG film. Impurities can be introduced by ion implantation. The impurities can include at least one element selected from the group consisting of argon, boron, nitrogen, and phosphorus.

In a method of manufacturing a semiconductor device according to a further aspect of the present invention, a conductive layer is formed on a substrate. On the conductive layer, a film is provided including at least 1 material selected from the group consisting of silicon oxide, silicon nitride, Ti, TiN, W, WN_X and TiW for substantially preventing intrusion of impurities implanted from above of the conductive layer into the conductive layer. The conductive layer and the intrusion prevention film are patterned. A first insulation film is formed on the patterned conductive layer and intrusion prevention film. Impurities are implanted into the first insulation film. This implantation of impurities into the first insulation film on the patterned conductive layer provides the advantage of improving the water resistance of the first insulation film. The provision of the intrusion prevention film on the conductive layer prevents intrusion of impurities into the conductive layer even when

impurities are implanted into the first insulation film. The problem of a shorter electromigration lifetime for the conductive layer (a Shorter Mean Time To Failure) caused by intrusion of the impurities into the conductive layer can be eliminated. Furthermore, planarization of the first insulation film is improved by employing an SOG film, for example, as the first insulation film. Thus, a semiconductor device can easily be manufactured that allows improvement of both planarization and water resistance.

The foregoing and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view of a semiconductor device according to an embodiment of the present invention.

Figs. 2-9 are sectional views of a semiconductor device of Fig. 1 for describing the manufacturing process.

Figs. 10-15 are diagrams of characteristics for describing the embodiment of the present invention.

Fig. 16 is a sectional view of a conventional semiconductor device for describing problems encountered in conventional art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of the present invention will be described hereinafter with reference to the drawings.

Referring to Fig. 1, a semiconductor device according to an embodiment of the present invention has a LOCOS (Local Oxidation of Silicon) film 2 for element isolation formed at a predetermined region on a main surface of a silicon substrate 1. A gate electrode 3 is formed on the main surface of the silicon substrate 1. A silicon oxide film 4 is formed so as to cover LOCOS film 2, gate electrode 3, and the surface of silicon substrate 1. A patterned metal interconnection 5 is formed on silicon oxide film 4 with a predetermined distance. A spacer 6 is formed on the upper surface of metal interconnection 5. A silicon oxide film 7 is formed so as to cover silicon oxide film 4, metal interconnection 5, and spacer 6. An organic SOG film 8 is formed on silicon oxide film 7. Argon ions (Ar^+)9 are implanted at a predetermined portion of organic SOG film 8. The portion of organic SOG film 8 where argon ions 9 are implanted is modified into an SOG film that does not include any organic component and that includes only a slight amount of moisture and hydroxyl group (referred to as "modified SOG film" hereinafter) 8a.

In the present embodiment, organic SOG film 8 can be modified partially or completely into modified SOG film 8a

by implanting argon ions (Ar^+)9 which is one type of impurities into organic SOG film 8 superior in planarization. Thus, planarization and water resistance can both be improved. Furthermore, by providing spacer 6 between metal interconnection 5 and organic SOG film 8a into which argon ions are implanted, the argon ions cannot enter metal interconnection 5 even when argon ions 9 are implanted into organic SOG film 8. Thus, the disadvantage that the lifetime of metal interconnection 5 up to disconnection caused by intrusion of impurities such as argon ions into metal interconnection 5 can be prevented. This issue will be described in details afterwards.

The manufacturing process of the semiconductor device of Fig. 1 (steps 1-8) will be described hereinafter with reference to Figs. 2-9.

According to the first step of Fig. 2, silicon oxide film 4 is formed approximately 300-800nm in thickness on the surface of a p type single crystalline silicon substrate 1 having the plane orientation of (100). This silicon oxide film 4 is formed so as to cover the gate electrode (not shown) and the like on silicon substrate 1. Silicon oxide film 4 can be formed by various methods such as oxidation, CVD, or PVD.

A metal interconnection layer 10 is formed on silicon oxide film 4 by magnetron sputtering. Metal

interconnection layer 10 has a stacked layer structure of TiN (film thickness 20nm)/Ti (film thickness 30nm)/AℓSiCu alloy (film thickness 500nm)/TiN (film thickness 100nm)/Ti (film thickness 50nm) in the downward direction.

A silicon oxide film 11 of approximately 200nm in film thickness is formed on metal interconnection layer 10 by plasma CVD. The gas used in plasma CVD includes monosilane and nitrous oxide (SiH_4+N_2O), monosilane and oxygen (SiH_4+O_2), TEOS (Tetra-Ethoxy-Silane : $Si(OC_2H_5)_4$) and oxygen ($TEOS+O_2$). The film growth temperature is 300-500°C. The film thickness of silicon oxide film 11 depends upon the underlying stepped portion.

The second manufacturing step will be described with reference to Fig. 3. Silicon oxide film 11 and metal interconnection layer 10 are etched simultaneously using the same photo resist mask (not shown). Accordingly, metal interconnection layer 10 and silicon oxide film 11 are formed as a metal interconnection 5 and a spacer 6, respectively. The etching process is carried out by, for example, reactive ion etching (RIE). Silicon oxide film 11 is etched using a gas including fluorine type gas (CF_4, CHF_3, and the like). Metal interconnection layer 10 is etched using a gas including chlorine type gas ($C\ell_2$, $BC\ell_3$, and the like).

In the third step shown in Fig. 4, silicon oxide film

7 is formed approximately 300nm in thickness by plasma CVD on the surface of the device formed by the previous second step. The film growth conditions of silicon oxide film 7 are similar to those of silicon oxide film 11.

At the fourth step shown in Fig. 5, organic SOG film 8 is formed on silicon oxide film 7. The composition of organic SOG film 8 is $[CH_3Si(OH)_3]$. Organic SOG film 8 has a thickness of approximately 400nm when there is no under layer pattern.

Organic SOG film 8 is formed as follows. First, an alcohol type solution of silicon compound of the above-described composition (for example, IPA + acetone) is applied on silicon substrate 1 in droplets. The substrate is rotated for 20 seconds at the rotary speed of 2300 rpm. As a result, a coating of alcohol type solution is formed on silicon substrate 1. This alcohol type solution coating is formed to alleviate the stepped portion on silicon substrate 1 by being formed thick at the concave portion and thin at the convex portion. As a result, the surface of the alcohol solution coating is planarized.

Then, in an atmosphere of nitrogen, a heat treatment is sequentially applied for 1 minute at 100°C, for 1 minute at 200°C, for 1 minute at 300°C, for 1 minute at 222°C, and for 30 minutes at 300°C. By this sequential heat treatment, the alcohol system is vaporized and polymerization

proceeds. An organic SOG film is formed having a planarized surface of approximately 200nm in thickness. By repeating the process starting from the coating formation to the heat treatment once more, organic SOG film 8 having a film thickness of approximately 400nm is obtained. At least 1% of C (carbon) is contained in organic SOG film 8 formed as described above.

At the fifth step shown in Fig. 6, argon ions (Ar^+) are doped into organic SOG film 8 by ion implantation. This implantation of impurity ions into the organic SOG film causes decomposition of the organic component in organic SOG film 8 as well as reduction of the moisture and the hydroxyl group included therein. As a result, the portion of organic SOG film 8 where impurity ions are implanted is modified into SOG film 8a that does not include any organic component and that includes only a slight amount of moisture and hydroxyl group.

Since the SOG film is employed as an interlayer insulation film of the interconnections here, there is a case where a via hole opening the upper portion of metal interconnection 5 is formed in this SOG film by dry etching at a subsequent step. When an SOG film that does not have ions implanted is dry etched, the surface exposed to etching is highly hygroscopic, resulting in increase in the amount of moisture and hydroxyl group at the area

exposed to etching. This increase of moisture at the area exposed to etching in an SOG film (the inner surface of the via hole) causes the disadvantage of corrosion of the upper metal interconnection connected to metal interconnection 5 through the via hole.

The side surface portion of metal interconnection 5 is still covered with silicon oxide film 7 even after formation of the via hole. This means that the side surface of metal interconnection 5 is isolated from the moisture and hydroxyl group included in the SOG film by silicon oxide film 7. Therefore, modification of organic SOG film 8 at least at the region located on the upper surface of metal interconnection 5 becomes critical in the present embodiment.

In view of the foregoing, the conditions of ion implantation must be set so that the thickest portion of the organic SOG film deposited on the upper surface of metal interconnection layer 5 is sufficiently modified. An acceleration energy of 140KeV and dosage of $1\times10^{15}/cm^2$ are employed as the ion implantation conditions here.

For the sake of simplifying the description, metal interconnection 5 is formed on an underlayer that is completely planer in Figs. 2 - 9. However in practice, the unevenness caused by each element formed on silicon substrate 1 affects silicon oxide film 4 in the

semiconductor process. As a result, metal interconnection 5 is not actually formed on a completely planer surface. More specifically, metal interconnection 5 is formed on an underlying interlayer insulation film (silicon oxide film 4) that has an uneven surface as shown in Fig 1. When there is no spacer 6 in the structure of Fig. 1, the structure of Fig. 16 is achieved. In the structure of Fig. 16, the film thickness of organic SOG film 8 (portion A) on the upper surface of metal interconnection 5 formed on an underlying concave surface differs from the film thickness of organic SOG film 8 (portion B) on the upper surface of metal interconnection 5 formed on an underlying convex surface. If ions are implanted under the condition for improving the film property of portion A, the ions will be implanted through inorganic SOG film 8 and silicon oxide film 7 at portion B to arrive at metal interconnection 5. This is undesirable since the reliability of metal interconnection 5 is degraded. This problem will be described in details hereinafter.

Fig. 10 shows the measured results of the average time for disconnection of a metal wiring formed of a stacked layer structure of TiN/Ti/AlSiCu/TiN/Ti when various ions are implanted. Measurement was carried out under the conditions of a current density of $3\times10^{6}A/cm^{2}$, a substrate temperature of 250°C, an interconnection width of

4μm, and an interconnection length of 1000μm. The absolute value was obtained with the measured value of the interconnection with no ions implanted as 1.

It is appreciated from Fig. 10 that the average time for disconnection becomes shorter by implanting ions into the AℓSiCu alloy layer in the interconnection. The result was particularly significant when argon (Ar), fluorine (F), and boron fluoride (BF_2) is used.

It is generally difficult to fill the silicon oxide film with no gaps where the spacing between interconnections is small since the step coverage of a silicon oxide film formed by plasma CVD is limited. There is a disadvantage that a void is generated in this spacing to adversely affect the reliability of the element.

An approach can be considered to prevent impurity ions from arriving at metal interconnection 5 by providing a thick silicon oxide film 7. However, there is a possibility that a void will be formed after formation of silicon oxide film 7 or organic SOG film 8 when the spacing between metal interconnection 5 is small if silicon oxide film 7 is made too thick. There is a disadvantage that increasing the thickness of silicon oxide film 7 does not commensurate with the rule of reducing the size of the interconnection.

In the present embodiment, spacer 6 is provided on

the upper surface of metal interconnection layer 5 instead of increasing the thickness of silicon oxide film 7. Spacer 6 effectively prevents the impurity ions from arriving at the AlSiCu alloy layer of metal interconnection 5 where the upper film of organic SOG film 8 is thin (refer to portion B in Fig. 16) even when ion implantation is set as one of the conditions for modifying organic SOG film 8 of a great thickness.

The portion of organic SOG film 8 located at the side surface of metal interconnection 5 does not necessarily have to be modified since the side surface of metal interconnection 5 is covered with silicon oxide film 7. However, this portion of organic SOG film 8 may be modified.

At the sixth step shown in Fig. 7, silicon oxide film 12 of approximately 200nm in thickness is formed on modified SOG film 8a by plasma CVD. The formation conditions of silicon oxide film 12 are similar to those of the above-described silicon oxide films 7 and 11.

At the seventh step shown in Fig. 8, anisotropic etching is carried out using mixture gas of carbon tetrafluoride and hydrogen as etching gas to form a via hole 13 connecting with metal interconnection 5.

At the eighth step, the interior of via hole 13 is cleaned by sputter etching using inert gas (such as Ar).

A TiN/Ti is deposited on a silicon oxide (not shown). Then, a tungsten (W) film (not shown) is formed on TiN and in via hole 13 by blanket tungsten CVD. By etching back this tungsten film until the silicon oxide film is exposed, a tungsten plug 14 as shown in Fig. 9 is formed within via hole 13.

Then, an Aℓ alloy film (Aℓ-Si(1%)-Cu(0.5%)) (film thickness 500nm), a Ti film (film thickness 50nm) and a TiN film (film thickness 20nm) are sequentially formed upwards within via hole 13 and on silicon oxide film 12 by magnetron sputtering. Using the general lithography and dry etching method (such as RIE), a resist (not shown) is applied, exposed, and etched. The aluminum alloy film, the Ti film and the TiN film are patterned to a predetermined configuration to form upper layer metal interconnection 15. Thus, metal interconnection 5 and upper layer metal interconnection 15 are electrically connected through tungsten plug 14.

Fig. 11 shows the result of an experiment carried out employing the structure using spacer 6 of the present embodiment under the conditions similar to those of Fig. 10. It is appreciated from Fig. 11 that the average time for disconnection of metal interconnection 5 is not shortened even when the step of implanting ions into organic SOG film 8 is employed. This means that the

reliability of metal interconnection 5 is not degraded even when impurities are implanted into organic SOG film 8 by virtue of spacer 6.

Since silicon oxide film 7 formed by plasma CVD can be as thin as possible by the provision of spacer 6, the spacing can easily be filled with silicon oxide film 7 even when the interconnection interval is reduced. This means that generation of a void is obviated.

Fig. 15 shows the results of an experiment carried out to verify whether there is change in the ion intrusion prevention effect of the interconnection by provision of spacer 6.

As a specimen, a plasma TEOS oxide film (PE-TEOS) of a substance identical to that of spacer 6 is formed on the interconnection of a TiN (film thickness 140nm)/Aℓ (film thickness 400nm)/TiN/Ti structure. Boron ions are implanted into this PE-TEOS under the conditions of an acceleration energy of 140KeV and dosage of $1\times10^{15}/cm^2$.

The MTTF (Mean Time To Failure) of the interconnection (average lifetime) with various film thicknesses of PE-TEOS was measured. The measurement was carried out at a current density of $3\times10^{16}A/cm^2$ and a substrate temperature of 250°C.

It is appreciated from Fig. 15 that the MTTF of the interconnection is increased as PE-TEOS becomes thicker.

This means that the PE-TEOS (spacer 6) is effective for preventing intrusion of ions, proportional to increase of the film thickness of spacer 6. The value of MTTF shows no more change when the film thickness of PE-TEOS becomes greater than 200nm. This is because intrusion of ions is effectively inhibited when the film thickness is greater than 200nm.

In the present embodiment, an interlayer insulation film of a three-layered structure of silicon oxide film 7, modified SOG film 8a and silicon oxide film 12 is employed for the purpose of further improving the insulation and the mechanical strength of the entire interlayer insulation film. The reason thereof will be described hereinafter.

In general, a silicon oxide film formed by plasma CVD is less hygroscopic and more water resistant than an organic SOG film. However, there is a phenomenon that the hygroscopic property is slightly increased by implanting ions into the silicon oxide film. It is to be noted that the silicon oxide film is significantly less hygroscopic than the organic SOG film, even if slightly increased. The fact that the underlying silicon oxide film 7 has a slightly higher hygroscopic property is of no problem since there is a modified SOG film 8a at the upper layer that has low hygroscopic property and high water

resistance. However, upper layer metal interconnection 14 is adversely affected if silicon oxide film 12 located above modified SOG film 8a becomes more hygroscopic. Silicon oxide film 12 should have a hygroscopic property as low as possible. In the present embodiment, silicon oxide film 12 is formed after implanting ions into organic SOG film 8 to prevent ions from being implanted into silicon oxide film 12. This prevents increase in the hygroscopic property of silicon oxide film 12.

The etching step of forming via hole 13 can be carried out in the atmosphere of a mixture gas of carbon tetrafluoride and hydrogen since no organic component is included in modified SOG film 8a. Therefore, a photo resist, when used as an etching mask, will not be affected in the etching process. This means that modified SOG film 8a masked with the photo resist is not etched. Therefore, a small via hole 13 can be formed accurately.

Furthermore, since modified SOG film 8a includes no organic components, the etching rate of modified SOG film 8a is equal to that of silicon oxide films 7, 11 and 12. Modified SOG film 8a will not shrink in the ashing process of removing the photo resist used as an etching mask. Furthermore, no cracks will be generated in modified SOG film 8a. Generation of a recess in forming via hole 13 can be prevented effectively. Thus, via hole 13 can be

sufficiently filled with tungsten plug 14.

As described above, modified SOG film 8a includes no organic components and includes only a slight amount of moisture and hydroxyl group. Also, no cracks are generated after the modification. Therefore, either or both of the underlying silicon oxide film 7 or the overlying silicon oxide film 12 of modified SOG film 8a can be omitted.

Fig. 12 shows the results evaluated by subjecting organic SOG film 8 (non-processed: unimplanted) and modified SOG film 8a (ion implantation process: Ar^+-implanted) respectively subjected to heat treatment for 30 minutes in a nitrogen ambient according to TDS (Thermal Desorption Spectroscopy). The ion implantation conditions are 140KeV for the acceleration energy and 1×10^{15}atoms/cm^2 for the dosage.

Fig. 12 shows the amount of desorption for H_2O (m/e=18). It is appreciated from Fig. 12 that desorption of H_2O (m/e=18) is small for modified SOG film 8a. This means that the moisture and the hydroxyl group included in organic SOG film 8 are reduced by modifying SOG film 8 into modified SOG film 8a by implanting Ar ions into organic SOG film 8.

Fig. 13 shows the results of an experiment carried out for the purpose of detecting the hygroscopic property of organic SOG film 8 and modified SOG film 8a. Organic

SOG film 8 (UNTREATED), an organic SOG film 8 exposed to oxygen plasma (O_2 plasma), and modified SOG film 8a (Ar+) are left in the air in a clean room. The amount of the moisture in each film was indicated by the area strength of the absorption (in the proximity of $3500cm^{-1}$) of the O-H group in the infrared absorption spectrum using the FT-IR method (Fourier transform infrared spectroscopy). The ion implantation conditions include the acceleration energy of 140KeV, and a dosage of $1\times10^{15}atoms/cm^2$.

It is appreciated from Fig. 13 that the moisture increases not only before and after the treatment, but also even after 24 hours (1 day) when exposed to oxygen plasma (O_2 plasma). In contrast, modified SOG film 8a (Ar^+) shows no moisture increase after ion implantation. The increase in moisture is smaller than that of organic SOG film 8 even when left in the air in a clean room. In other words, modified SOG film 8a is less hygroscopic than organic SOG film 8.

Fig. 14 shows the results of a pressure cooker test (PCT) carried out for the purpose of detecting the moisture permeability of modified SOG film 8a and organic SOG film 8. This pressure cooker test is a humidification test carried out in a saturated steam ambient at 2 atmospheric pressure and 120°C in the present embodiment. The area intensity of the absorption peak (in the vicinity

of 3500cm^{-1}) of the O-H in organic SOG film 8 was obtained and plotted over the PCT time using FT-IR method.

A specimen (Ar^+20KeV) having only the surface modified by ion implantation was prepared and compared with a specimen having the film entirely modified (Ar^+140KeV) and with a specimen that was not modified (organic SOG film 8: untreated). When organic SOG film 8 not modified is subjected to the pressure cooker test, the absorption intensity in the vicinity of 3500cm^{-1} (of the O-H group) shows a significant increase. In modified SOG film 8a, increase of the absorption intensity in the vicinity of 3500cm^{-1} (of the O-H group) is small. The increase in the specimen having only the film surface modified is equal to that of the film that is completely modified.

It is understood from the above results that a layer that has moisture permeability suppressed can be formed by implanting ions.

The present invention is not limited to the above-described embodiment, and similar effects and advantages can be obtained by the following implementation.

(1) At least one of modified SOG film 8a and silicon oxide film 12 is etched back entirely, or polished by chemical•mechanical polishing (CMP), for example, after one or all the fourth to sixth steps. This provides the

advantage of increasing planarization of the film. In this case, it is preferable to preset the film thickness to a slightly thick value and obtain a predetermined thickness by etching back or by polishing.

(2) A material that prevents the implanted ions from arriving at the AℓSiCu alloy in metal interconnection 5 such as a silicon nitride film, refractory metal such as titanium and tungsten, or refractory metal compound is used instead of silicon oxide film 11 (spacer 6). Particularly, the usage of refractory metal and compound thereof is advantageous in that the reliability of the interconnection and the contact is improved due to the conductance thereof.

Titanium is typical of refractory metal. Refractory metal also includes molybdenum, tungsten, tantalum, hafnium, zirconium, niobium, vanadium, rhenium, chromium, platinum, iridium, osmium, and rhodium.

(3) The TiN/Ti layer used as the uppermost layer of metal interconnection 5 can be commonly used as a spacer 6 instead of silicon oxide film 11 (spacer 6). In this case, the TiN/Ti layer must be set to a film thickness that sufficiently prevents ions from arriving at the AℓSiCu alloy in metal interconnection 5. A single layer of Ti, TiN, W, WN_X or TiW, or a multilayer thereof can be used instead of the TiN/Ti layer.

(4) Ions are implanted into the inorganic SOG film used as an alternative to organic SOG film 8. In this case, the moisture and hydroxyl group included in the inorganic SOG film can be reduced.

(5) A silicon oxide film can be used that is formed other than by plasma CVD (atmospheric pressure CVD, low pressure CVD, ECR plasma CVD, photo excited CVD, TEOS-CVD, PVD, etc.) instead of the silicon oxide films 7, 11 and 12 formed by plasma CVD.

(6) Although argon ions are employed as the ion to be implanted into organic SOG film 8 in the above-described embodiment, any ion that can modify organic SOG film 8 can be used. Specifically, ions that have relatively small masses such as argon ions, boron ions, nitrogen ions, or phosphorus ions are suitable. The following ions also can be expected to have a competent effect. For example, helium ions, neon ions, krypton ions, xenon ions, and radon ions which are inert gas ions besides argon can be considered. Inert gas is advantageous in that there is no possibility of the elements being adversely affected by ion implantation since inert gas does not react with organic SOG film 8.

Furthermore, element unitary ions of the group IIIb, IVb, Vb, VIb, and VIIb other than boron and nitrogen, and compound ions thereof can be used. Particularly, the

element unitary ions and compound ions of oxygen, aluminum, sulfur, chlorine, gallium, germanium, arsenic, selenium, bromine, antimony, iodine, indium, tin, tellurium, lead, and bismuth can be used. Particularly, metal element ions can suppress the dielectric constant to a low level of organic SOG film 8 subjected to ion implantation.

Furthermore, element unitary ions of groups Ⅳa, Ⅴa, and compound ions thereof can be used. Particularly, element unitary ions of titanium, vanadium, niobium, hafnium, and tantalum, and compound ions thereof can be considered. Since the dielectric constant of the oxides of the element of the groups Ⅳa, Ⅴa is high, the dielectric constant of organic SOG film 8 subjected to ion implantation increases. However, this is of no particular problem in practice except for cases where an interlayer insulation film of low dielectric constant is required.

A plurality of the types of the above-described ions can be used in combination. In this case, a further superior effect can be obtained by the synergism of each ion.

(7) In the above-described embodiment, ions are implanted into organic SOG film 8. The present invention is not limited to ions, and a similar effect can be obtained by injecting atoms, electrons, molecules, or particles having kinetic energy. In the present invention,

these are generically referred to as "impurities".

(8) The sputtering method is not limited to magnetron sputtering. Diode sputtering, radio frequency sputtering, tetrode sputtering, and the like can be employed.

(9) Reactive ion beam etching (also called RIBE or reactive ion milling) using reactive gas (for example $CC\ell_4$, SF_6) besides the usage of inert gas can be employed for sputtering etching.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first insulation film formed on a conductive layer, and including impurities, and

a film formed between said first insulation film and said conductive layer for substantially preventing intrusion of said impurities into said conductive layer.

2. The semiconductor device according to claim 1, wherein said intrusion prevention film includes at least one material selected from the group consisting of silicon oxide, silicon nitride, Ti, TiN, W, WN_X and TiW.

3. The semiconductor device according to claim 1, further comprising a second insulation film formed between said first insulation film and said conductive layer.

4. The semiconductor device according to claim 3, wherein said second insulation film includes a film less hygroscopic than said first insulation film.

5. The semiconductor device according to claim 1, wherein said first insulation film includes silicon oxide containing at least 1% of carbon.

6. The semiconductor device according to claim 1, wherein said first insulation film includes an inorganic SOG film.

7. The semiconductor device according to claim 1, wherein said impurities include at least one element selected from the group consisting of argon, boron, nitrogen, and phosphorus.

8. The semiconductor device according to claim 1, wherein an upper surface of said first insulation film is planarized.

9. A method of manufacturing a semiconductor device comprising the steps of:

forming a first insulation film on a conductive layer formed on a substrate,

introducing impurities into said first insulation film, and

forming a film to substantially prevent the impurities introduced into said first insulation film from entering said conductive layer prior to said step of forming said first insulation film.

10. The manufacturing method of a semiconductor

device according to claim 9, wherein said intrusion prevention film includes at least one material selected from the group consisting of silicon oxide, silicon nitride, Ti, TiN, W, WN_X and TiW.

11. The method of manufacturing a semiconductor device according to claim 9, further comprising the step of forming a second insulation film on said conductive layer and said intrusion prevention film prior to said step of forming the first insulation film.

12. The method of manufacturing a semiconductor device according to claim 11, wherein said second insulation film includes a film less hygroscopic than said first insulation film.

13. The method of manufacturing a semiconductor device according to claim 9, further comprising the step of forming a third insulation film on said first insulation film after said step of implanting impurities into the first insulation film.

14. The method of manufacturing a semiconductor device according to claim 9, wherein said first insulation film includes silicon oxide containing at least 1% of

carbon.

15. The method of manufacturing a semiconductor device according to claim 9, wherein said first insulation film includes an inorganic SOG film.

16. The method of manufacturing a semiconductor device according to claim 9, wherein said step of introducing impurities is carried out by ion implantation.

17. The method of manufacturing a semiconductor device according to claim 9, wherein said impurities include at least one element selected from the group consisting of argon, boron, nitrogen, and phosphorus.

18. A method of manufacturing a semiconductor device comprising the steps of:

forming a conductive layer on a substrate,

forming a film on said conductive layer, said film including at least one material selected from the group consisting of silicon oxide, silicon nitride, Ti, TiN, W, WN_X and TiW, for substantially preventing impurities implanted from above of said conductive layer from intruding into said conductive layer,

patterning said conductive layer and said intrusion

prevention film,

forming a first insulation film on said patterned conductive layer and intrusion prevention film, and

implanting impurities into said first insulation film.

ABSTRACT OF THE DISCLOSURE

A semiconductor device including an insulation film superior in both planarization and water resistance is obtained. In this semiconductor device, a first insulation film including impurities is formed on a conductive layer. A film is formed between the first insulation film and the conductive layer for substantially preventing impurities from entering the conductive layer. Water resistance of the first insulation film is improved since impurities are included in the first insulation film. By using an insulation film superior in planarization as the first insulation film, a first insulation film superior in both planarization and water resistance can be obtained. The film provided between the first insulation film and the conductive layer prevents the impurities of the first insulation film from entering the conductive layer. Therefore, reduction in the reliability of the conductive layer can be prevented.

FIG.1

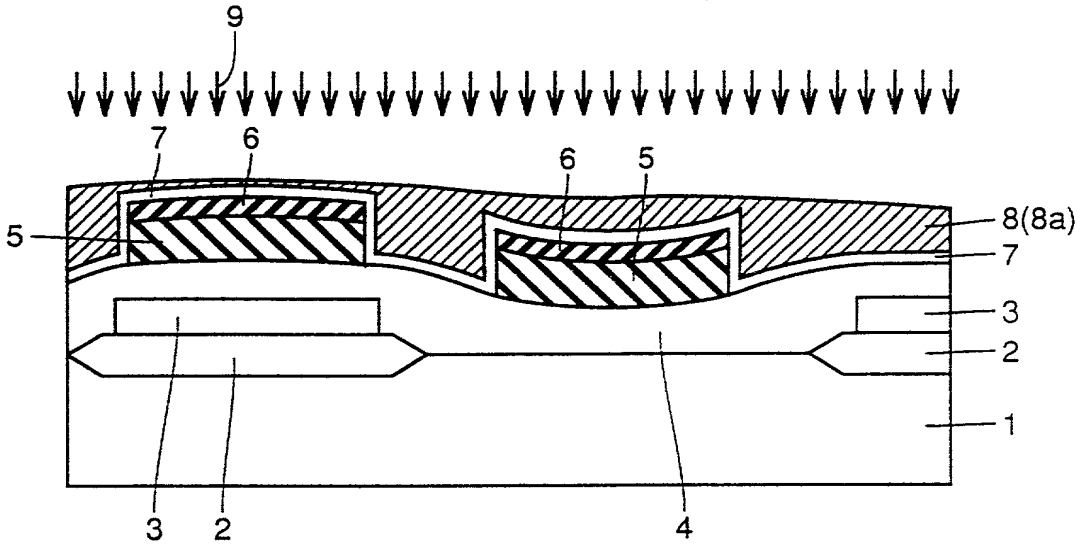


FIG.2

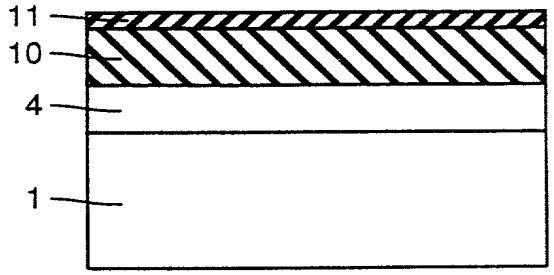


FIG.3

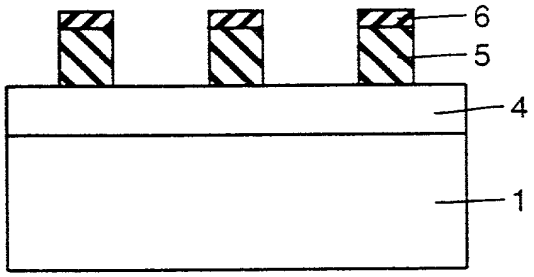


FIG.4

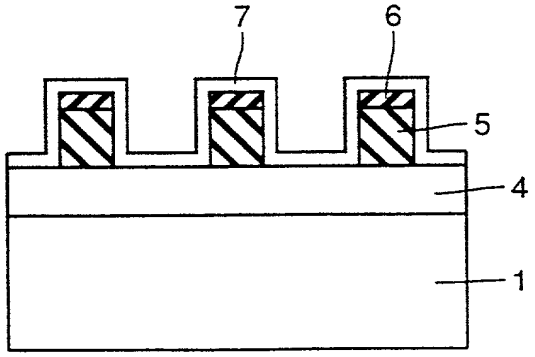


FIG.5

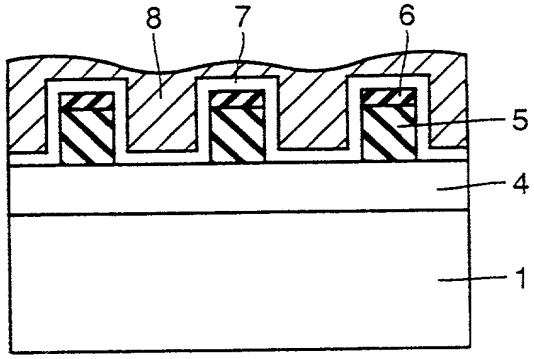


FIG.6

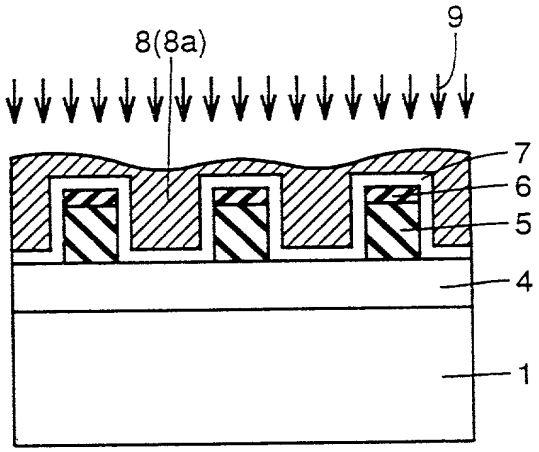


FIG.7

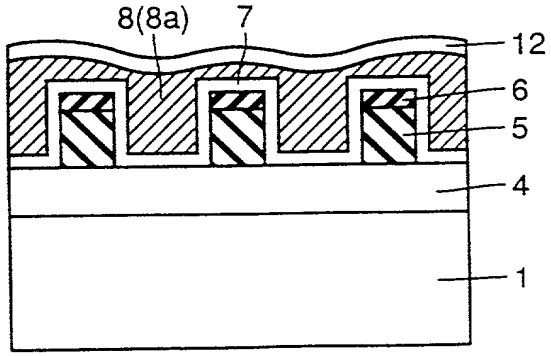


FIG.8

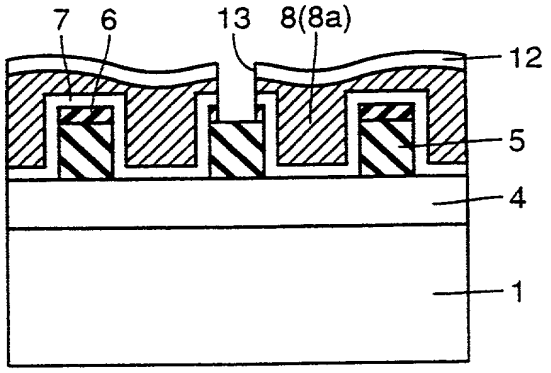


FIG.9

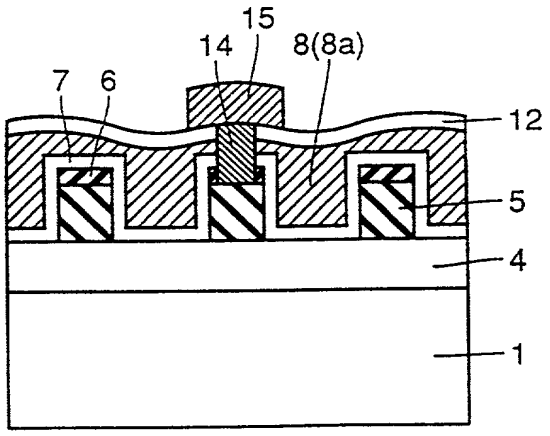


FIG.10

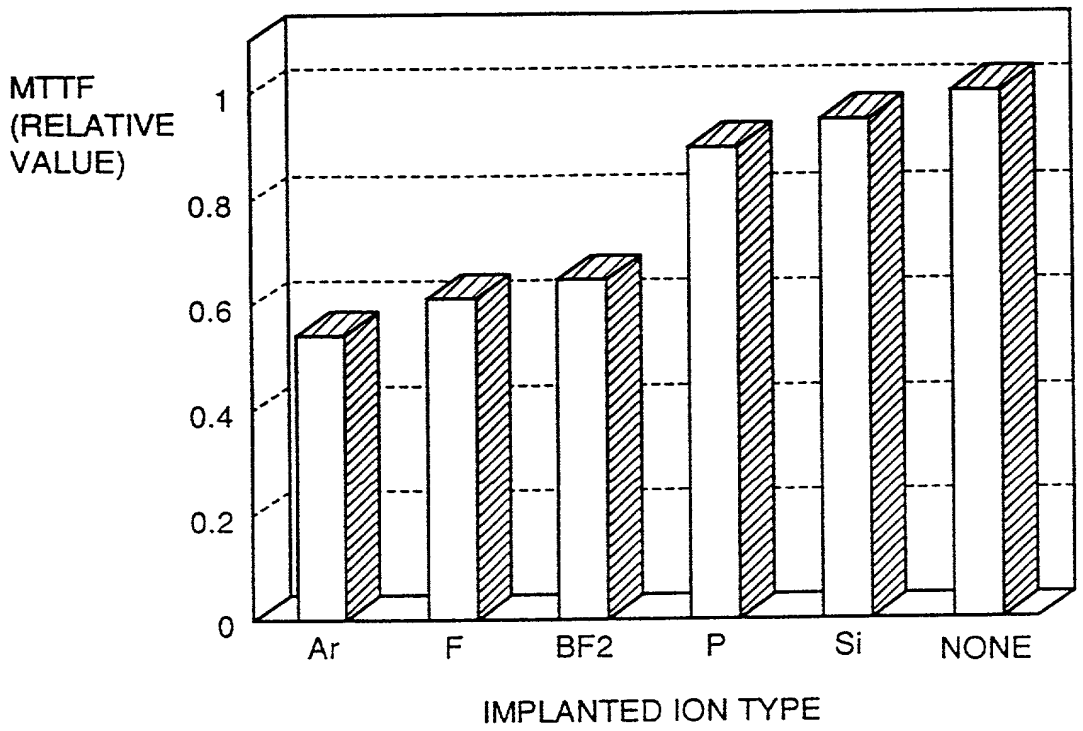
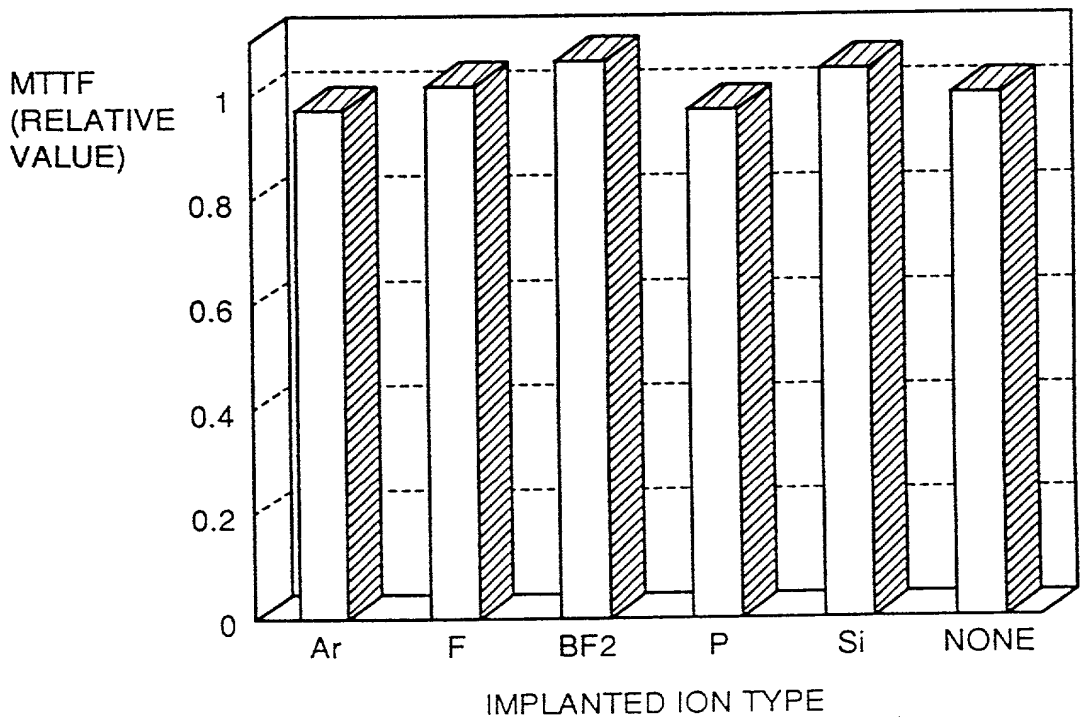

MTTF
(RELATIVE
VALUE)
1
0.8
0.6
0.4
0.2
0
Ar
F
BF2
P
Si
NONE
IMPLANTED ION TYPE

FIG.11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(RELATIVE
VALUE)
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0.4
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Ar
F
BF2
P
Si
NONE
IMPLANTED ION TYPE

FIG.12

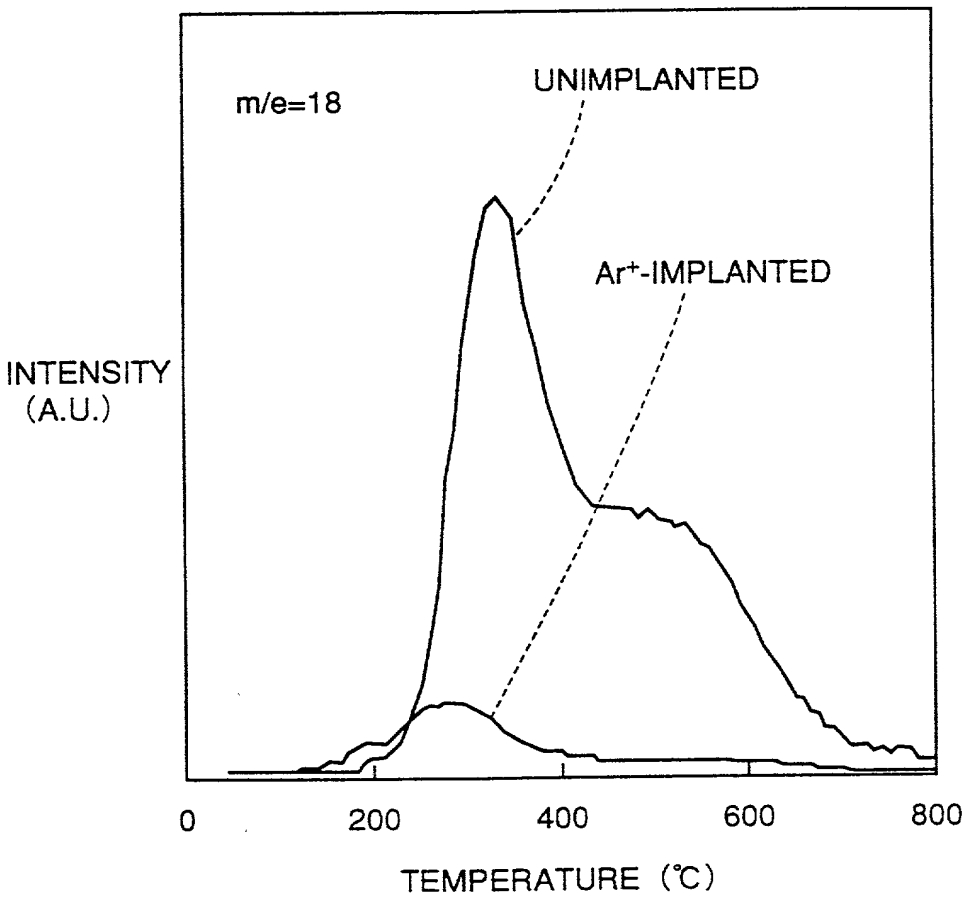
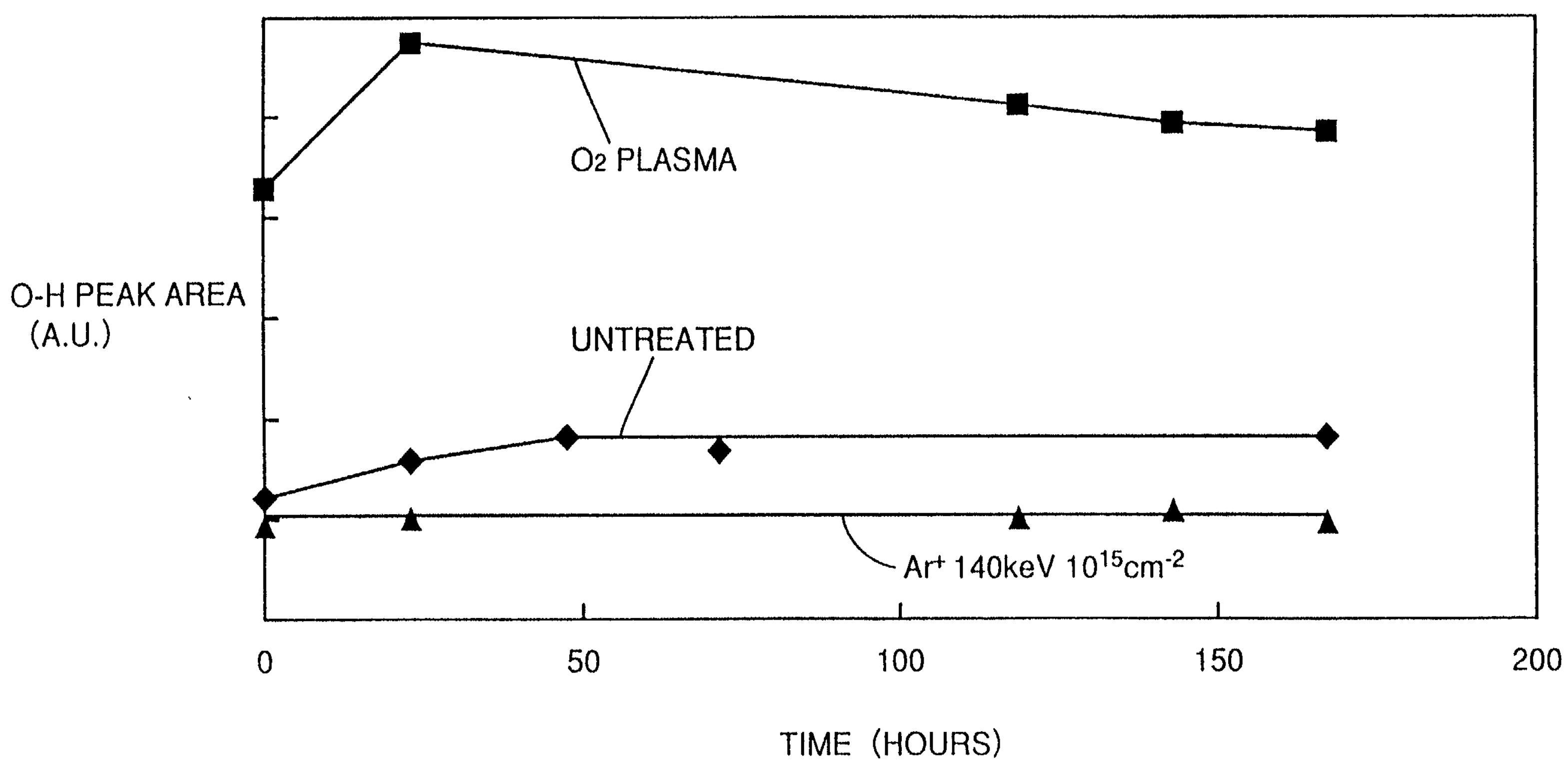
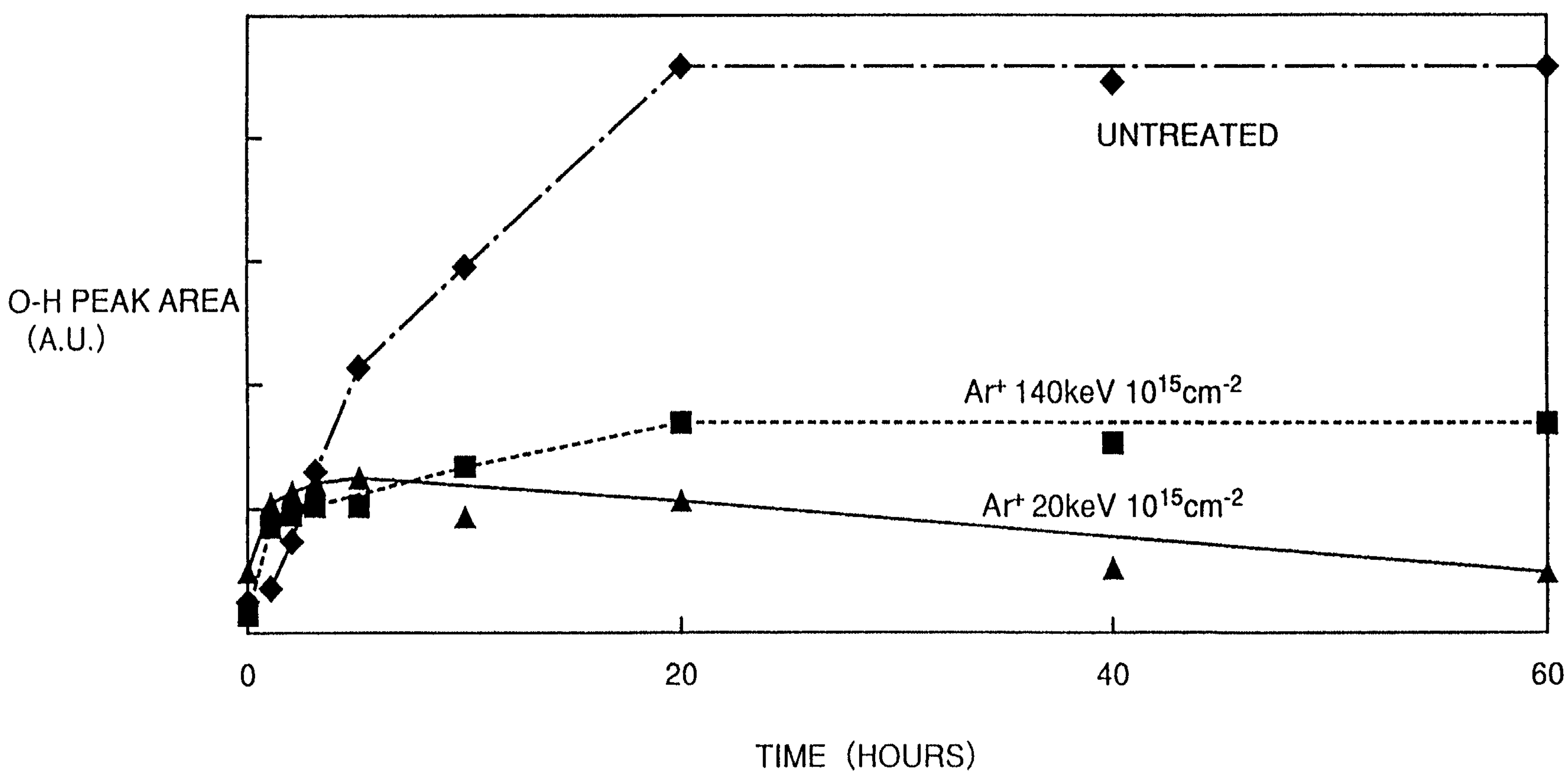

m/e=18
UNIMPLANTED
Ar+-IMPLANTED
INTENSITY
(A.U.)
0
200
400
600
800
TEMPERATURE (℃)

FIG.13



O-H PEAK AREA
(A.U.)
O2 PLASMA
UNTREATED
Ar+ 140keV 10^15cm^-2
0
50
100
150
200
TIME (HOURS)

FIG.14



UNTREATED
Ar+ 140keV 10^15cm^-2
Ar+ 20keV 10^15cm^-2
O-H PEAK AREA
(A.U.)
0
20
40
60
TIME (HOURS)

FIG.15

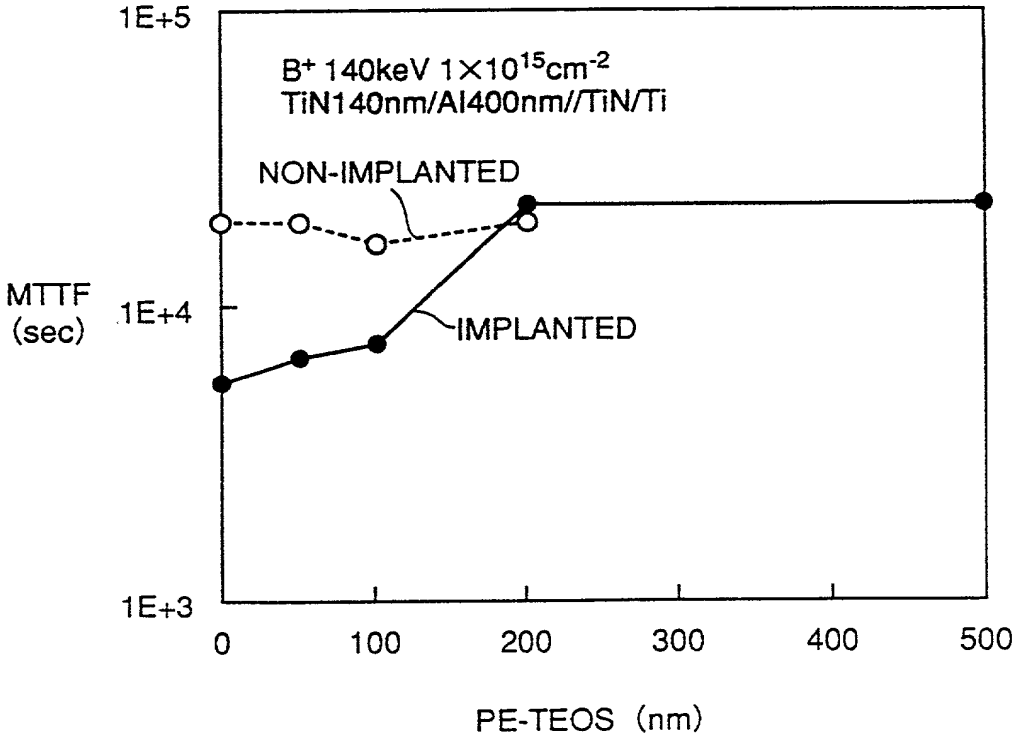
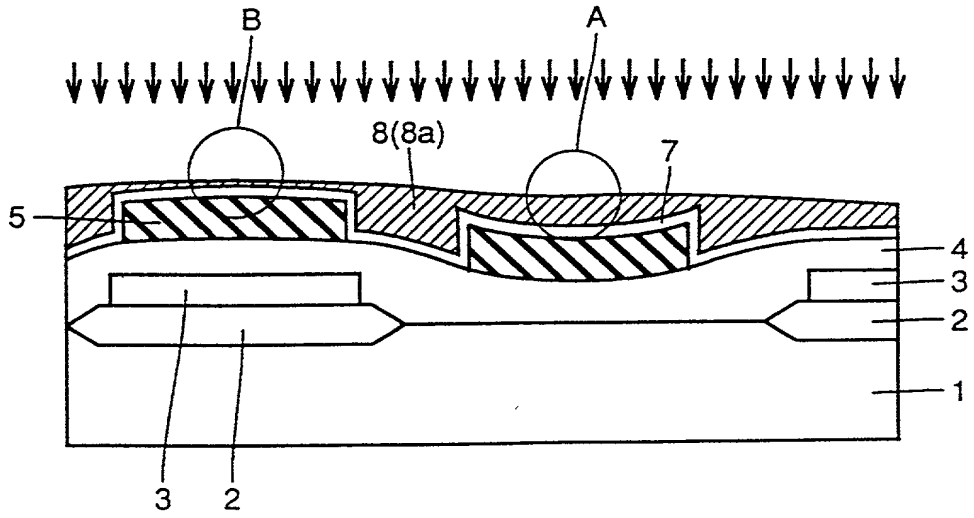

1E+5
B+ 140keV 1×10^15cm^-2
TiN140nm/Al400nm//TiN/Ti
NON-IMPLANTED
MTTF
(sec)
1E+4
IMPLANTED
1E+3
0
100
200
300
400
500
PE-TEOS (nm)

FIG.16


B
A
8(8a)
7
5
4
3
2
1
3
2

Docket No. _____

ARMSTRONG, WESTERMAN, HATTORI, McLELAND & NAUGHTON

DECLARATION FOR NEW U.S. PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled Semiconductor Device Including an Insulation Film on a Conductive Layer and Manufacturing Method Thereof The specification of which

(Check one of blocks 1, 2 or 3.)

1. ☒ is attached hereto.
2. ☐ was filed on _____ as International PCT Application Serial No. _____ and was amended on _____ (if applicable)
3. ☐ was filed on _____ U.S. Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specificating, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application as defined in Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application for which priority is claimed.

(Number)	(Country)	(Day/Month/Year Filed)	Priority Claimed
8-43679(P)	Japan	29/February/1996	X Yes __ No
9-12788(P)	Japan	27/January/1997	X Yes __ No
			__ Yes __ No
			__ Yes __ No

___ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1,56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

Cont'd.--

Rev.#3, 10/92

List Prior U.S. Applications:

(Appln. Serial No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)
(Appln. Serial No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)
(Appln. Serial No.)	(Filing Date)	(Status: Patented, Pending, Abandoned)

And I hereby appoint as principal Attorneys James E. Armstrong, III, Reg. No. 18,366; William F. Westerman, Reg. No. 29,988; Ken-Ichi Hattori, Reg. No. 32,861; John R. Pegan, Reg. No. 18,069; William G. Kratz, Jr., Reg. No. 22,631; Le-Nhung McLeland, Reg. No. 31,541; James P. Welch, Reg. No. 17,379; Ronald F. Naughton, Reg. No. 24,616; Albert Tockman, Reg. No. 19,722; J. Herbert O'Toole, Reg. No. 31,404; Mel R. Quintos, Reg. No. 31,898; Michael J. Foycik, Jr., Reg. No. 30,928; Mary E. Gormley, Reg. No. 34,409; James C. Lydon, Reg. No. 30,082; Vivian P. Kafalenos, Reg. No. 32,903; Donald W. Hanson, Reg. No. 27,133,; Stephen G. Adrian, Reg. No. 32,878; Gregory R. Muir, Reg. No. 35,293; William L. Brooks, Reg. No. 34,129; Joseph J. Zito, Reg. No. 32,076.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature Yasunori Inoue Date February 17, 199
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Inventor's signature Hideki Mizuhara Date February 17, 199
Residence Aichi, Japan
Citizenship Japanese
Post Office Address 34-1-201, Aza-Yuukuno, Higashiitsushiro, Bisai-shi, Aichi, Japan

Full name of third joint inventor, if any _____
Inventor's signature _____ Date _____
Residence _____
Citizenship _____
Post Office Address _____

Full name of fourth joint inventor, if any _____
Inventor's signature _____ Date _____
Residence _____
Citizenship _____
Post Office Address _____

Full name of fifth joint inventor, if any _____
Inventor's signature _____ Date _____
Residence _____
Citizenship _____
Post Office Address _____

Contd.--